What is claimed is:

1. A data transfer control system for transferring data through a bus, comprising:

a command processing section which receives a command packet transferred through a first bus and issues a command included in the command packet to a device connected with a second bus; and

a Direct Memory Access (DMA) transfer instruction section which sets a fixed DMA data length irrespective of type of the issued command and instructs start of DMA transfer to or from the device connected with the second bus.

2. The data transfer control system as defined in claim 1,

wherein the DMA transfer instruction section aborts the started DMA transfer when the device which is connected with the second bus and has received the issued command informs of completion of command processing.

3. The data transfer control system as defined in claim 1,

wherein the DMA transfer instruction section instructs start of the DMA transfer when the device which is connected with the second bus and has received the issued command requests start of the DMA transfer.

4. The data transfer control system as defined in claim 1,

wherein the device connected with the second bus is a device which writes data transferred through the second bus in a storage or reads data to be transferred through the second bus from the storage, and

wherein the DMA transfer instruction section sets a value greater than a storage capacity of the storage as the fixed DMA data length.

5. The data transfer control system as defined in claim 1,

wherein the DMA transfer instruction section sets a value greater than a data length which is capable of being designated by a command included in the command packet as the fixed DMA data length.

6. The data transfer control system as defined in claim 1,

wherein the command processing section issues a command included in the command packet to the device connected with the second bus without decoding the command.

7. The data transfer control system as defined in claim 1,

wherein the first bus is a bus through which data is transferred according to a first interface standard and the second bus is a bus through which data is transferred according to a second interface standard, and

wherein the command packet is a packet defined by a higher layer protocol of the first interface standard.

8. The data transfer control system as defined in claim 1,

wherein the first bus is a bus through which data is transferred according to the IEEE1394 standard and the second bus is a bus through which data is transferred according to the AT Attachment (ATA)/ATA Packet Interface (ATAPI) standard, and

wherein the command packet is an ORB packet defined by the Serial Bus Protocol-2 (SBP-2).

9. An electronic instrument comprising:

the data transfer control system as defined in claim 1; and

the device connected with the second bus.

10. A program causing a data transfer control system to function as:

a command processing section which receives a command packet transferred through a first bus and issues a command included in the command packet to a device connected with a second bus; and

a Direct Memory Access (DMA) transfer instruction section which sets a fixed DMA data length irrespective of type of the issued command and instructs start of DMA transfer to or from the device connected with the second bus.

11. The program as defined in claim 10,

wherein the DMA transfer instruction section aborts the started DMA transfer when the device connected with the second bus which has received the issued command informs of completion of command processing.

12. A data transfer control method for transferring data through a bus, the method comprising:

receiving a command packet transferred through a first bus and issuing a command included in the command packet to a device connected with a second bus; and

setting a fixed Direct Memory Access (DMA) data length irrespective of type of the issued command and instructing start of DMA transfer to or from the device connected with the second bus.

13. The data transfer control method as defined in claim 12, further comprising:

aborting the started DMA transfer when the device connected with the second bus which has received the issued command informs of completion of command processing.

14. The data transfer control method as defined in claim 12, further comprising:

instructing start of the DMA transfer when the device connected with the second bus which has received the issued command requests start of the DMA transfer.

15. The data transfer control method as defined in claim 12,

wherein the device connected with the second bus is a device which writes data transferred through the second bus in a storage or reads data to be transferred through the second bus from the storage, and

wherein the method further comprises setting a value greater than a storage capacity of the storage as the fixed DMA data length.

16. The data transfer control method as defined in claim 12, further comprising:

setting a value greater than a data length which is capable of being designated by a command included in the command packet as the fixed DMA data length.

17. The data transfer control method as defined in claim 12, further comprising:

issuing a command included in the command packet to the device connected with the second bus without decoding the command.

18. The data transfer control method as defined in claim 12,

wherein the first bus transfers data conforming to a first interface standard and the second bus transfers data conforming to a second interface standard, and

wherein the command packet is a packet defined by a higher layer protocol of the first interface standard.

19. The data transfer control method as defined in claim 12,

wherein the first bus transfers data conforming to the IEEE1394 standard and

the second bus transfers data conforming to the AT Attachment (ATA)/ATA Packet Interface (ATAPI) standard, and

wherein the command packet is an operation request block (ORB) packet defined by the Serial Bus Protocol-2 (SBP-2).

5